

**VLSI Design**  
B.E. Sem. VII [ETRX]

---

---

**EVALUATION SYSTEM**

	<b>Time</b>	<b>Marks</b>
<b>Theory Exam</b>	3 Hrs.	100
<b>Practical Exam</b>	–	–
<b>Oral Exam</b>	–	25
<b>Term Work</b>	–	25

**Objective :** To familiarize students with the different aspects of the VLSI field and to introduce important concepts that have industry value.

**Pre-requisite :** Digital System Design I and II, BEC.

**SYLLABUS**

**1. Introduction to VLSI**

Evolution of logical complexity in ICs as a function of time, VLSI design flow, Y-chart representation, design hierarchy/design abstraction levels in digital circuits, concepts of regularity, modularity and locality, Semi-custom & full custom devices.

**2. Physics of MOSFET**

MOS capacitor, energy band diagrams, band bending, flat band voltage, threshold voltage calculation, threshold adjustment, MOSFET linear and saturated operation(GCA), MOSFET capacitance, channel length modulation.

Types of scaling, functional limitations of scaling, short channel, narrow channel effects, hot electron effects.

**3. Semiconductor manufacturing process**

Wafer processing, mask generation, oxidation, epitaxy, ion implantation, diffusion, metallization, photolithography, process steps for NMOS & PMOS devices, CMOS inverters, latch-up in CMOS and its prevention. Process simulation using CAD tools Video of manufacturing process to be shown.

**4. Design rules and layout**

Need of design rules, NMOS, PMOS and CMOS design rules and layouts. Design of NMOS and CMOS Inverter, NAND and NOR gates. Interlayer contacts, Butting and Buried contacts. Stick diagrams, layout of integrated circuits. Realization of Boolean expressions in CMOS. Use of CAD tools for layout design and simulation.

**5. MOS Inverters**

MOS inverters - resistive load - NMOS load - pseudo NMOS (Qualitative) and CMOS inverters (quantitative) -calculation of noise margin, calculation of rise, fall and delay times for CMOS inverter, transistor sizing and power dissipation , series and parallel equivalency rules, equivalent inverter (numericals on noise margin calculations, timing calculations, power dissipation, equivalency expected)

**6. Verilog**

Basic concepts, structural gate level, switch level, behavior and RTL modeling. Arithmetic Circuits in CMOS VLSI – carry look ahead adder, high speed adders, subtractors, decoders, multiplexer and multipliers. Sequential circuits' implementation using verilog (Flip-Flop, registers and counters, state machines).

---

**References :**

1. CMOS Digital Integrated Circuits - Analysis & Design (*Sung-Mo Kang & Yusuf Leblebici*) Second Ed., MGH
2. Digital Integrated Circuits - A Design Perspective (*Jan M Rabaey*) Prentice Hall
3. Introduction to VLSI Design (*Fabricius, Eugene D.*) TMH
4. A Guide to Digital Design and Synthesis (*Samir Palnitkar, Verilog HDL*) Pearson Education.
5. Principles of CMOS VLSI Design : A System Perspective (*Neil H.E. Weste, Kamran Eshraghian*) Addison Wesley publication.
6. Fundamentals of Modern VLSI Devices (*Yuan Taur*) Cambridge University Press.

