Digital System Design – I

S.E. Sem. III [ETRX]

EVALUATION SYSTEM

	Time	Marks
Theory Exam	3 Hrs	100
Practical Exam	3 Hrs.	25
Oral Exam	–	25
Term Work	–	25

SYLLABUS

1. **Introduction and Digital Codes**
   Analog Vs Digital Systems, Digital Devices, Binary codes, Gray codes, Character codes, Codes for detecting and correcting errors.

2. **Logic Circuits**
   Boolean Algebra, theorems, combinational circuit analysis, combinational circuit synthesis, minimization, Karnaugh Map, Sum of Products, Product of Sums form and their minimization, Programmed minimization-Quine Mc-Cluskey minimization algorithm, timing hazards-static, Dynamic Hazards.

3. **Combinational MSI, LSI Devices**
   Combinational design using SSI, MSI devices, Decoders (74 × 139, 74 × 138), Encoders (74 × 148), Tri-state buffers (74 × 244, 74 × 245), Multiplexers (74 × 151), Parity circuits (74180), Comparators (7485), Adders (7483), Subtractors, BCD adders–subtractors, ALU (74181), Combinational Multipliers, Combinational PLDs.

4. **Logic families**
   Basics of TTL, CMOS, ECL Circuits for basic logic operations just Circuits and working of them in all above families. No Characteristics of families.

5. **Sequential Logic Practices**
   Basic Elements, Latches and Flip-Flops, S-R, D.T., J-K latches and Flip-Flops, Flip-Flop conversions, Applications of Latches and Flip-Flop in switch debouncing, bus holder circuits, Flip-Flop Timing Considerations and Metastability.

6. Counters – Asynchronous, Synchronous counters, UP-down counters, Mod counters, Ring counters, Shift Registers, Universal Shift register.

Reference :

1. Modern Digital Design (*RP Jain*) – fourth edition, Tata McGraw Hill.
2. Digital Design (*Morris Mano*) – Pearson Education, Asia, 2002.
3. Digital Design Principles and Practices (*John F. Wakerley*) third edition updated, Pearson Education, Singapore, 2002.
4. Digital Logic : Application and Design (*John M. Yarbrough*) – Thomson Brooks/Cole, 2004.

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