

Computer Organization and Architecture [COA]

S.E. Sem. III [CMPN]

EVALUATION SYSTEM

	Time	Marks
Theory Exam	3 Hrs.	100
Practical and Oral Exam	–	–
Oral Exam	–	–
Term Work	–	25

SYLLABUS

1. Basic structure of computer

Introduction of computer system and its sub modules, Basic organization of computer and block level description of the functional units. Von newmann model, Introduction to buses and connecting I/O devices to CPU and memory, Asynchronous and synchronous bus, PCI, SCSI.

2. Arithmetic and Logic Unit

Arithmetic and logical unit hardware implementation, Booth's Recoding, Booth's algorithm for signed multiplication, Restoring division and non restoring division algorithm, IEEE floating point number representation and operations.

3. Central Processing Unit

CPU architecture, Register organization, Instruction formats and addressing modes (Intel processor), Basic instruction cycle, Instruction interpretation and sequencing, Control Unit operation, Hardwired control unit design methods and design examples, Multiplier control unit, Micro programmed control unit, basic concepts, Microinstruction sequencing and execution, Micro operations, concepts of nanoprogramming, Introduction to RISC and CISC architectures, design issues and examples of RISC processors.

4. Memory Organization

Characteristics of memory system and hierarchy, concepts of semiconductor memories, main memory, ROM, EPROM, RAM, SRAM, DRAM, SDRAM, RDRAM, Flash memory, Stack Organization. High speed memories: Cache memory organization and mapping, replacement algorithms, cache coherence, Interleaved and associative memories, Virtual memory, main memory allocation, segmentation paging. Secondary storage. RAID optical memory, CDROM, DVD.

5. I/O Organization

Input/Output systems. Programmed I/O, Interrupt driven I/O, I/O channels, DMA, Peripheral Devices. U.S.B.

6. Multiprocessor Configurations

Flynn's classifications, parallel processing concepts. Introduction to pipeline processing and pipeline hazards, design issues of pipeline architecture. Instruction pipeline. Instruction level parallelism and advanced issues.

7. SPARC

Static and Dynamic data flow design, Fault tolerant computers, Interprocessor communication and synchronization, cache coherence, shared memory multiprocessor.

8. Systolic Architectures

Systolic arrays and their applications, wave front arrays.

References :

1. Computer Architecture and Organization (*Miles Murdocca*) – Wiley India.
2. Computer Organization and Architecture : Designing and performance (*William Stallings*) – Prentice – Hall India.
3. Computer Organization (*Carl Hamacher, Zvonko Vranesic and Safwat Zaky*) – McGraw Hill.
4. Computer Architecture A Quantitative Approach (*John L. Hennessy and David Patterosn*) – Morgan Kaufman.
5. Structured Computer Organization (*Andrew S. Tanenbaum*) – Prentice – Hall India.

